Powerized

Digitalization of Power Electronic Applications within Key Technology Value Chains

PROGRESS TO SUCCESS

UC3.1b Intelligent Gate Driver for Industrial Inverters

Lead: ABB Partners: TECHNISCHE UNIVERSITÄT DRESDEN, Infineon

Objectives / KPI

- Improved current balancing of hard paralleled IGBT / inverter modules
  (Goal: $\Delta I_{C,mean}$ < 1 % and i_C < 10% in forward direction)
- Ability to control the dv/dt (Goal: adjustment accuracy ≈ 1 kV/µs)
- Novel fully digital interfaced IPM including control and driver circuit with a higher density of control to power part by at least 50%

Methods

- Measuring and evaluating the output current
- Adjusting the turn-on and turn-off delay times
- Adjusting the IGBT-Gate voltage

Challenges

- Fast and and accurate control of the Gate voltage (suitable

Motivation

Control of switching properties

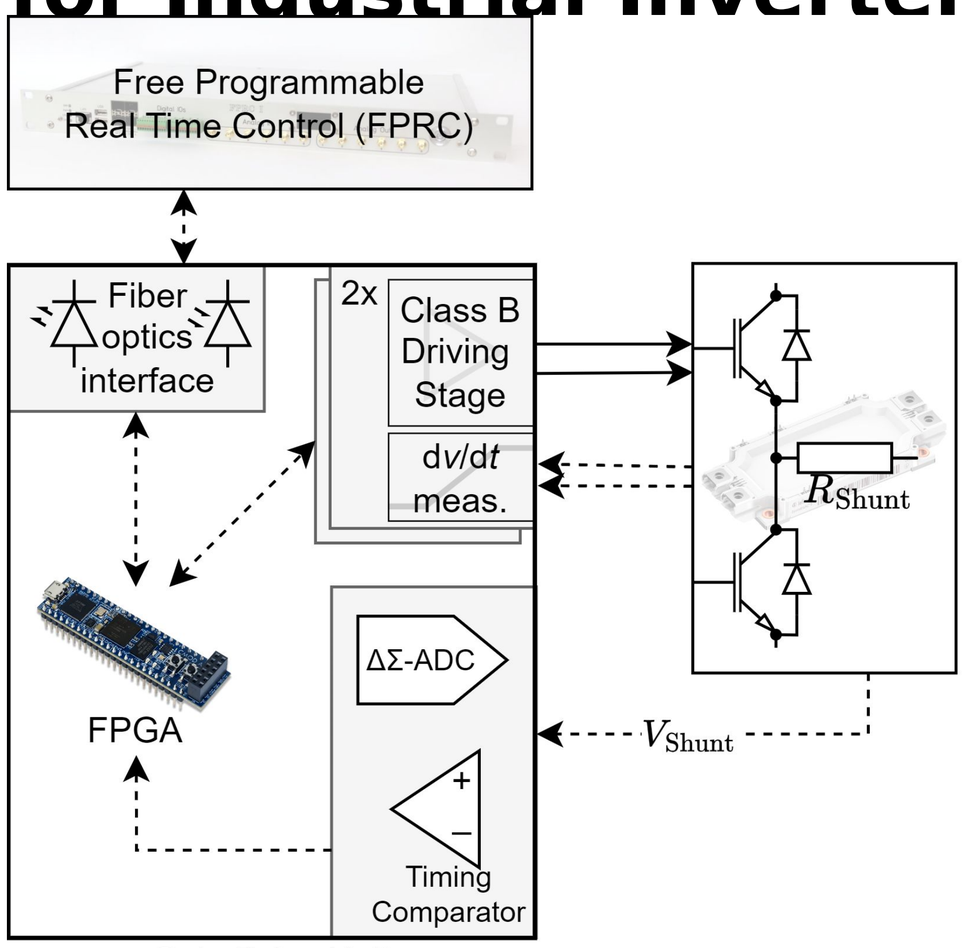
- State of the art: Output filter to limit the dv/dt for sensitive loads and EMC
  - Optimization for the worst-case operating point
- New approach: Control dv/dt for reduced filter requirements
  - Smaller filters → lower costs
  - Possibility to control dv/dt according to the operating point → lower losses

Intelligent parallel connection of modules

- State of the art: Characterization and selection of IGBTs
  - High economic and ecological costs
- New approach: Adjustment of the dynamic and static characteristics
  - Dynamic current balancing by controlling the length of the miller plateau
  - Static current balancing by control of the turn-on-voltage

Relevance

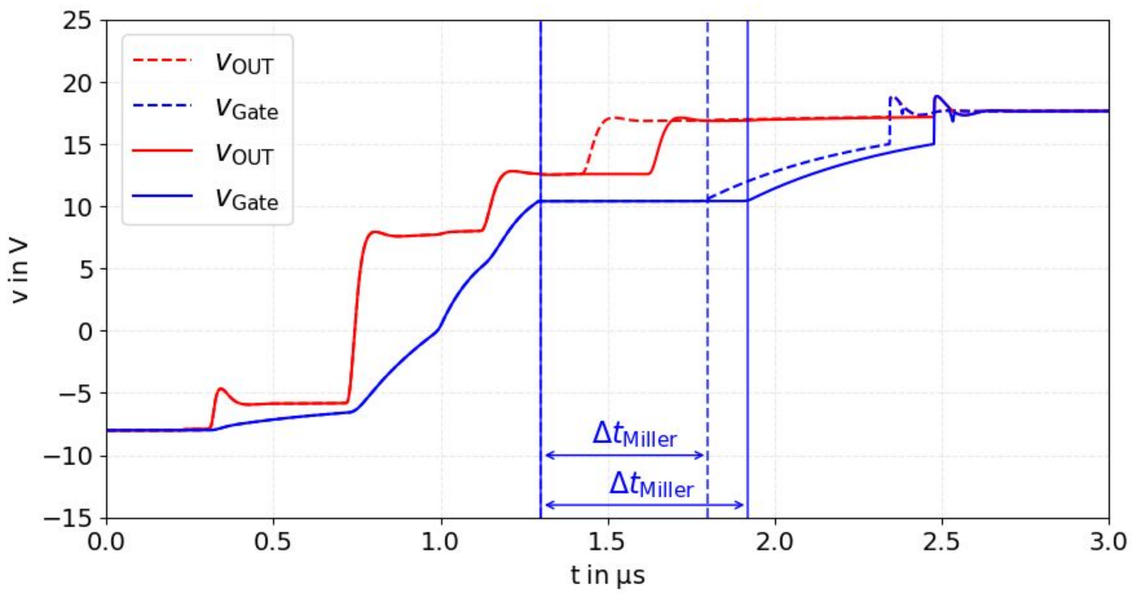
- Active control of the IGBT behavior → Possibility to parallel IGBTs with different characteristics → Improved second source policy
- Different online switching performance optimizations are possible → lower overall losses, lower EMC, ...



Simplified block-diagram of the Gate Driver functions

Image Sources: FPGA: https://digilent.com/shop/cmod-a7-35t-breadboardable-artix-7-fpga-module/
IGBT: Datasheet IFF750B12ME7
FPRC: https://converterlabs.de/docs/fprc

Comparison of different wafeforms at the output of the Class-B amplifier



Simulated Gate-Voltage-Control for dv/dt control and current balancing with two different control regimes for adjusting the length of the miller plateau (solid and dashed)

v_{OUT} ... Output voltage of the driver
v_{Gate} ... Gate-Emittter-Voltage IGBT

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